WHAT IS CLAIMED IS:

1. A liquid crystal display device including a data line supplied with a data signal, a gate line supplied with a scanning signal, a pixel electrode for driving a liquid crystal cell, and a thin film transistor for applying the data signal to the pixel electrode in response to the scanning signal, the device comprising:

a gate insulating film covering the gate line; and

a storage electrode at the interior of the gate insulating film to overlap with the gate line.

2. The liquid crystal display device according to claim 1, wherein a distance between the gate line and the storage electrode is about 500 to 2500Å.

3. The liquid crystal display device according to claim 1, further comprising:

a protective layer on the gate insulating film to cover the data line, the gate line and the thin film transistor.

4. The liquid crystal display device according to claim 3, wherein the pixel electrode is connected to the storage electrode via a contact hole passing through the gate insulating film and the protective layer.

5. A method of fabricating a liquid crystal display having a storage electrode, comprising:

forming a gate line and a gate electrode of a thin film transistor on a substrate;

depositing a first gate insulating film on the substrate to cover the gate electrode and the gate line;

forming the storage electrode on the first gate insulating film to overlap with the

gate line;

depositing a second gate insulating film on the first gate insulating film to cover the storage electrode;

forming an active layer and an ohmic contact layer on the gate insulating films;

forming a source electrode and a drain electrode of the thin film transistor opposed to each other having a desired channel therebetween on the ohmic contact layer;

forming a protective layer on the gate insulating film to cover the source electrode and the drain electrode;

defining a first contact hole exposing the drain electrode on the protective layer;

defining a second contact hole exposing the storage electrode on the protective layer and the second gate insulating film; and

forming a pixel electrode connected to the drain electrode, via the first contact hole, and connected to the storage electrode on the protective layer, via the second contact hole.

6. The method according to claim 5, wherein a distance between the gate line and the storage electrode is about 500 to 2500Å.

7. A liquid crystal display device comprising:

a gate line and a data line on a substrate to cross each other;

a thin film transistor including a gate electrode, a source electrode, and a drain electrode, and provided at an intersection between the data line and the gate line; and

a storage electrode at the interior of a gate insulating film and overlapping with the gate line.

8. The liquid crystal display device according to claim 7, further comprising a

gate insulating film formed on the substrate to cover the gate electrode and the gate line and to electrically isolate the gate line and the data line from each other.

9. The liquid crystal display device according to claim 8, further comprising an active layer and an ohmic contact layer formed on the gate insulating film to overlap with the gate electrode.

10. The liquid crystal display device according to claim 8, further comprising a protective layer formed on the gate insulating film to cover the gate line, the data line, and the thin film transistor.

11. The liquid crystal display device according to claim 7, wherein the gate electrode is connected to the gate line.

12. The liquid crystal display device according to claim 7, wherein the source electrode is connected to the data line.

13. The liquid crystal display device according to claim 12, wherein the drain electrode is opposed to the source electrode, and wherein a channel is formed between the source electrode and the drain electrode.

14. The liquid crystal display device according to claim 10, wherein a pixel electrode is connected to the drain electrode via a first contact hole provided on the protective layer.

15. The liquid crystal display device according to claim 10, wherein the storage capacitor includes a storage electrode and the gate line opposed to each other and having the gate insulating film formed therebetween.

16. The liquid crystal display device according to claim 15, wherein the storage electrode is connected to a transparent electrode pattern via a second contact hole.

17. A method of fabricating a liquid crystal display, comprising the steps of:

forming a gate line and a gate electrode of a thin film transistor on a substrate;

depositing a first gate insulating film on the substrate to cover the gate electrode and the gate line;

forming a storage electrode on the first gate insulating film to overlap with the gate line;

depositing a second gate insulating film on the first gate insulating film to cover the storage electrode;

forming an active layer and an ohmic contact layer on the gate insulating films;

forming a source electrode and a drain electrode of the thin film transistor opposed to each other having a desired channel therebetween on the ohmic contact layer;

forming a protective layer on the gate insulating film to cover the source electrode and the drain electrode;

forming a pixel electrode connected to the drain electrode; and

forming a transparent electrode pattern connected the storage electrode on the protective layer.

18. The method according to claim 17, further comprising:

defining a first contact hole for exposing the drain electrode on the protective layer; and

defining a second contact hole for exposing the storage electrode on the protective layer and the second gate insulating film.

19. The method according to claim 18, wherein the second contact hole is formed to the same thickness as the first contact hole by patterning the second gate insulating film using the protective layer as a mask to expose the storage electrode.

20. The method according to claim 17, wherein the gate electrode and the gate line are formed by depositing a metal from one of aluminum and copper using sputtering and then patterning the metal.

21. The method according to claim 17, wherein the first gate insulating film is formed by depositing an insulating material to a thickness of about 500 to 2500 Å using plasma enhanced chemical vapor deposition.

22. The method according to claim 21, wherein the second gate insulating film is formed to the same thickness of the first gate insulating film.

23. The method according to claim 17, wherein the first and second gate insulating films are formed from one of silicon nitride and silicon oxide.

24. The method according to claim 17, wherein the storage electrode is formed by depositing a metal from one of chromium and molybdenum using a technique from one of chemical vapor deposition and sputtering, and then patterning the metal.

25. The method according to claim 17, wherein the active layer and the ohmic contact layer are formed by depositing first and second semiconductor materials, respectively, after forming the gate insulating films, and then patterning the materials.

26. The method according to claim 25, wherein the first semiconductor material includes undoped amorphous silicon.

27. The method according to claim 25, wherein the second semiconductor material includes one of n-type and p-type amorphous silicon at a high concentration.

28. The method according to claim 17, wherein the source and drain electrodes are formed by depositing a metal layer from one of chromium and molybdenum using a technique from one of chemical vapor deposition or sputtering, and then patterning the metal.

29. The method according to claim 17, wherein the protective layer includes one of silicon nitride and silicon oxide.

30. The method according to claim 17, wherein the protective layer includes an organic insulating material having a small dielectric constant selected from one of acrylic organic compound, Teflon, benzocyclobutene, Cytop, and perfluorocyclobutane.

31. The method according to claim 17, wherein the pixel electrode and the transparent electrode pattern are formed by depositing a transparent conductive material from one of indium-tin-oxide, indium-zinc-oxide, and indium-tin-zinc-oxide on the protective layer and then patterning the transparent conductive material.